



A55F-M4 VER : A

ECS CONFIDENTIAL

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REVISION HISTORY:

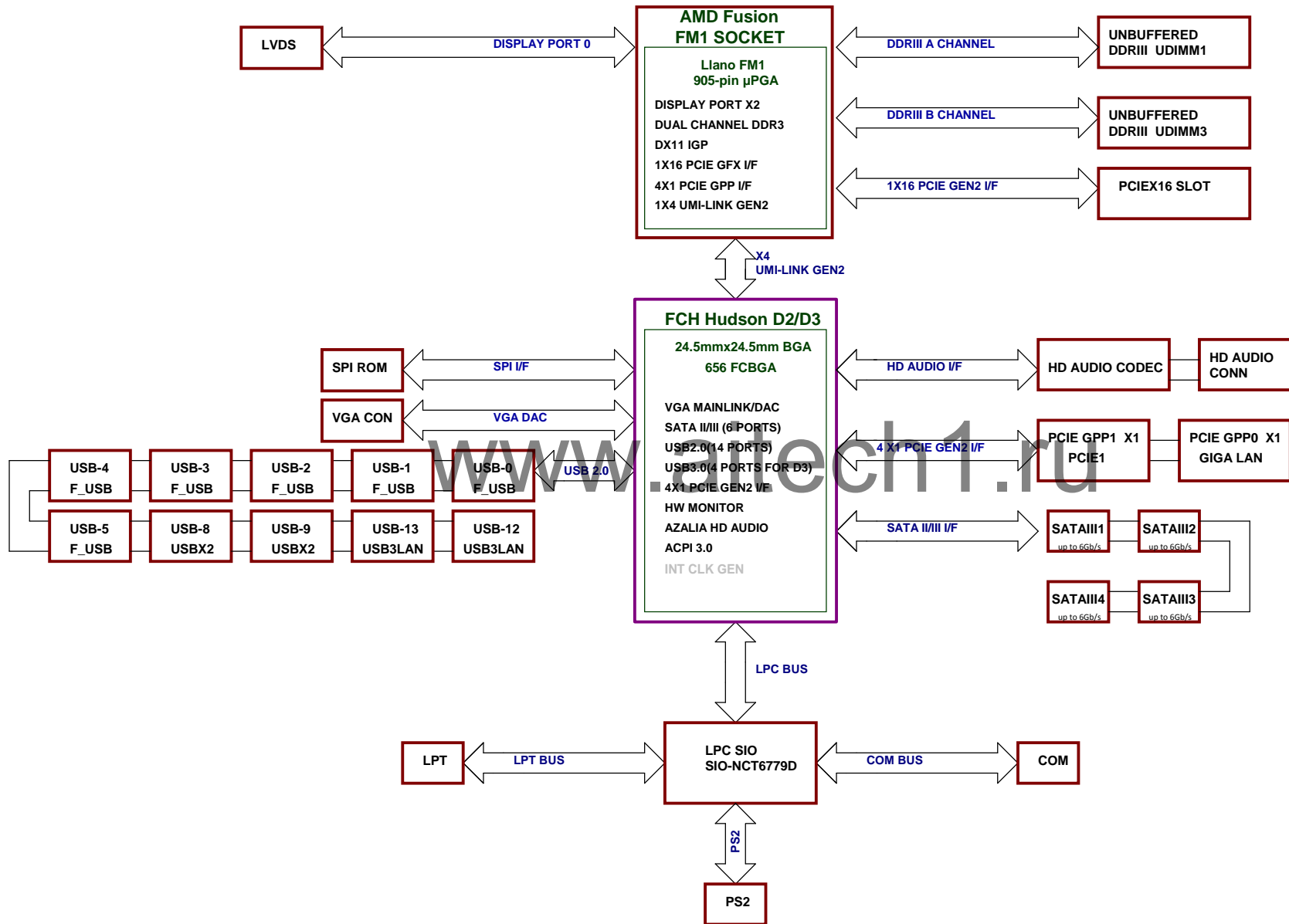
Page	Index	Rev	Date	Notes
20	RT8871&9619/VCORE	A	2011/08/19	Modify from A75F-M3
21	VDDR/VDDP/PCH CORE			
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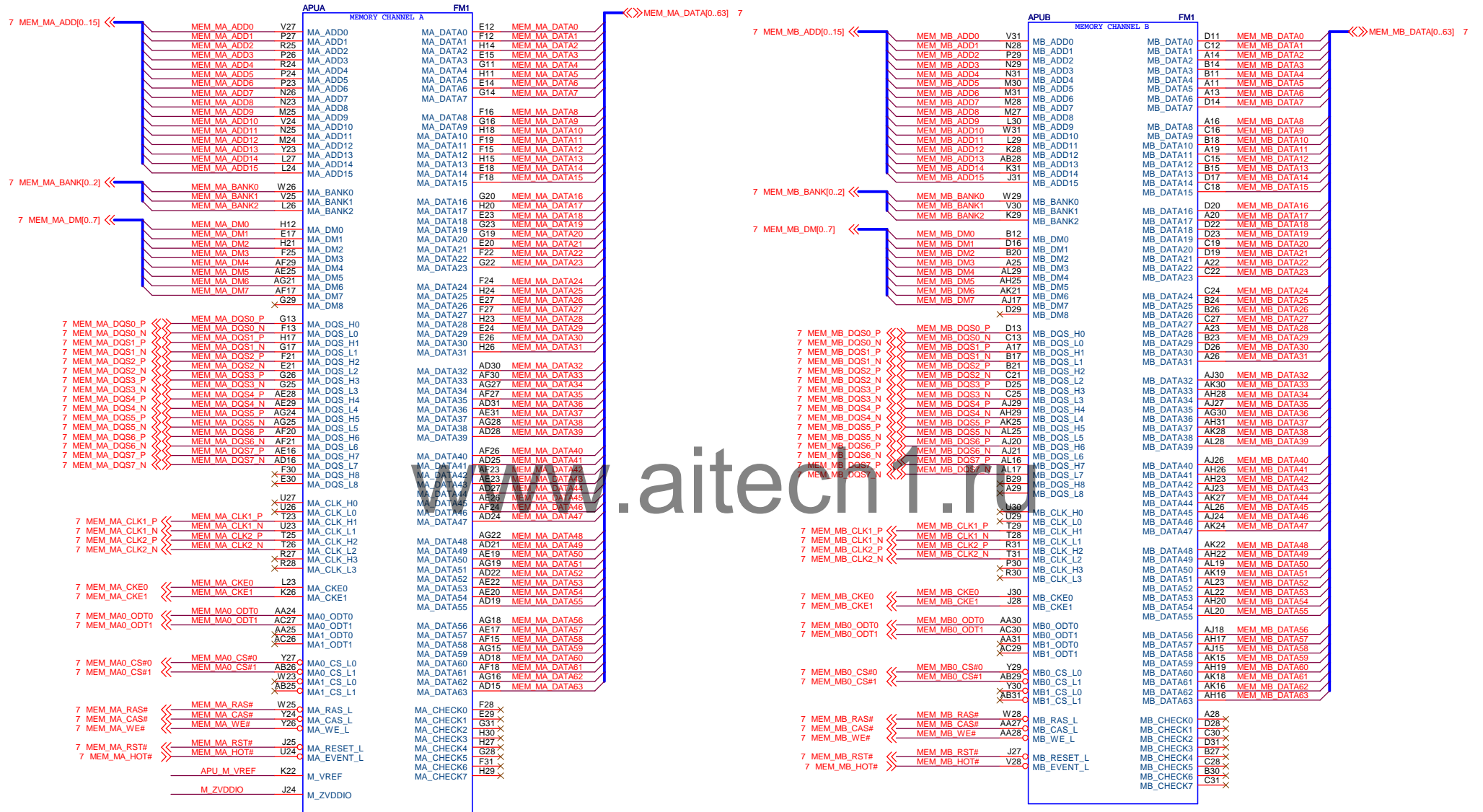
IMPORTANT NOTES ABOUT THIS SCHEMATIC

- DESIGN NOTE: Example 1) DESIGN NOTES in text for the design note to grey are information show the note inside the notes. colored box.
- DESIGN NOTE: Example 2) DESIGN NOTES in text for the design note to yellow are notes of show the note inside the caution. colored box.
- DESIGN NOTE: Example 3) DESIGN NOTES in text for the design note to red are critical, and show the note inside the must be understood and colored box. followed.

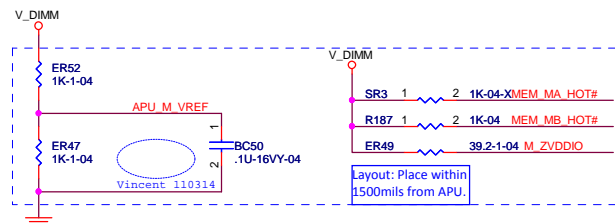
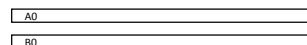
BLOCK DIAGRAM



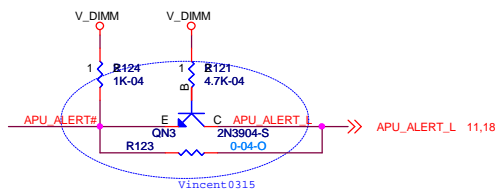
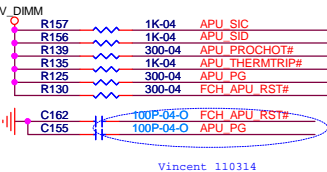
FM1 DDR3 MEMORY



Layout: DIMM Slots placement

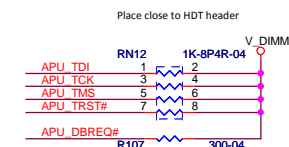
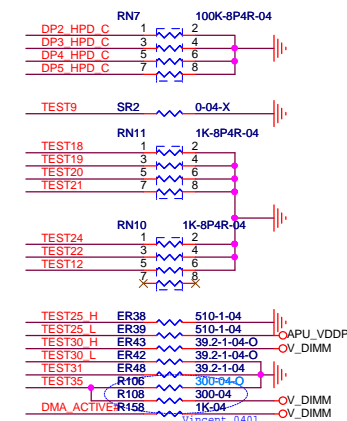
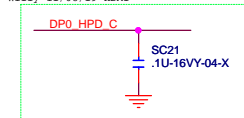


FM1 MEMORY		
Size Custom	Document Number	Rev A
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FM1R1: This pin should be pulled up to an "always on" supply voltage on the platform. The power should not be allowed to turn on if this pin is low. This pin acts as an electrical key which prevents physical damage if an incompatible part is inserted. Failure to pull this pin high, may result in permanent damage to the board and/or incompatible APU

Willy 11/08/19 HDMI

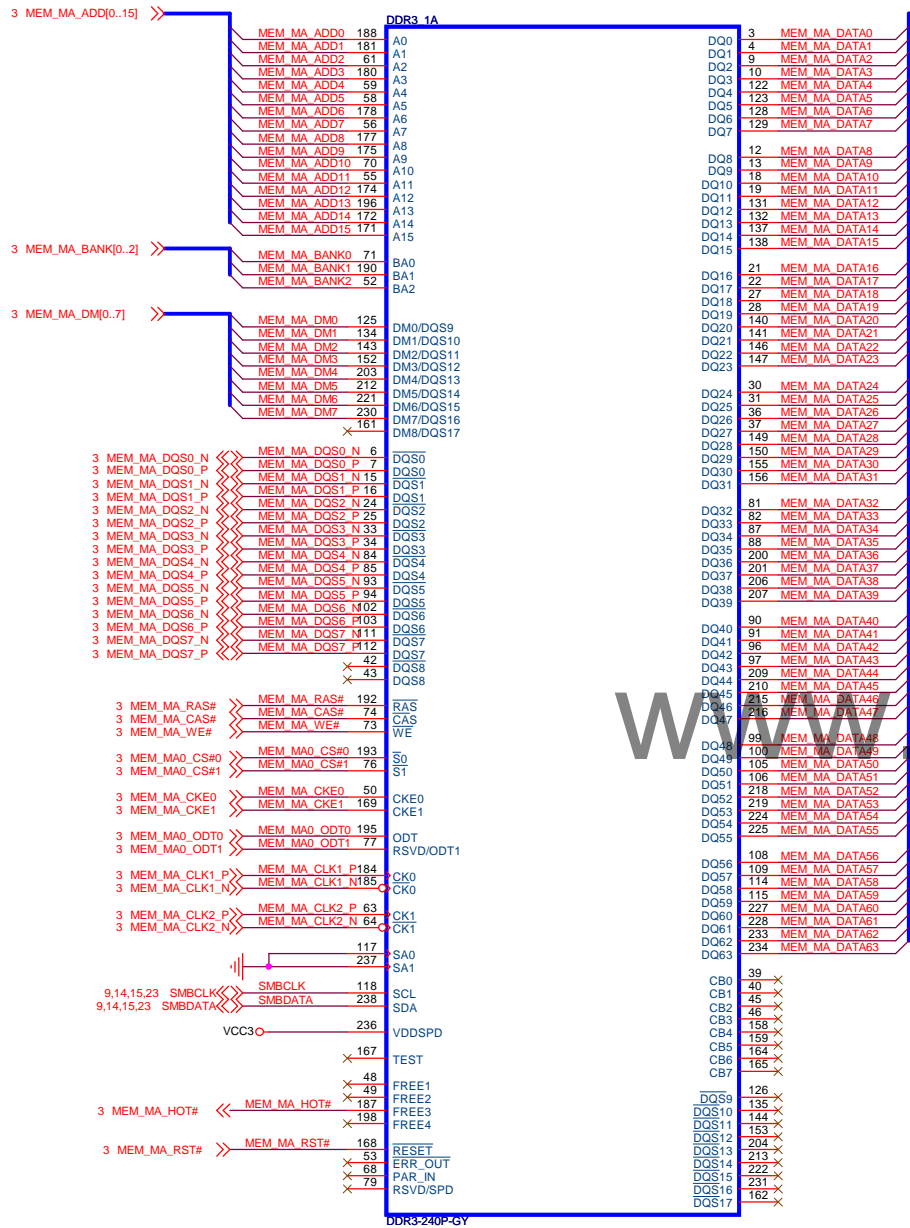


DEL:HDT hao 11/6/3

APUE



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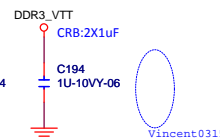
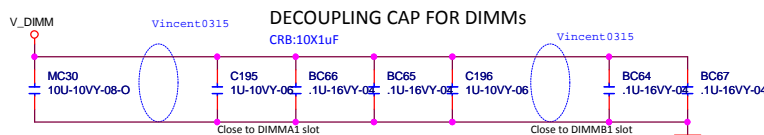
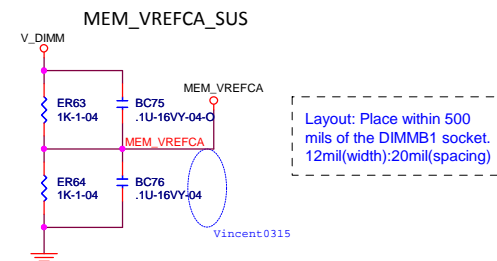
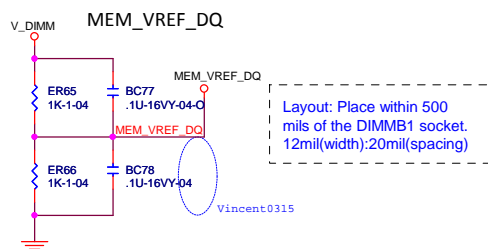
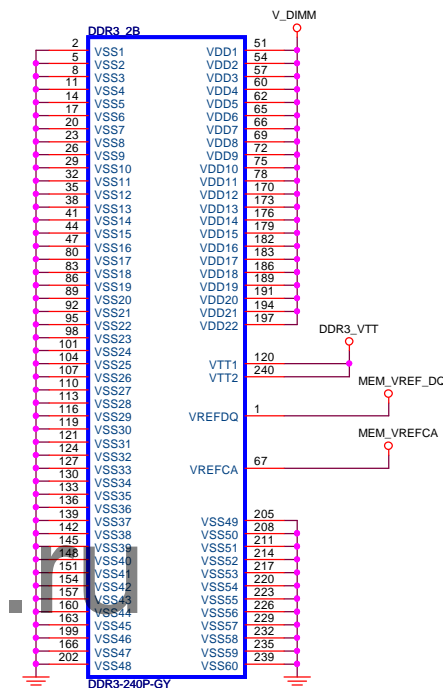
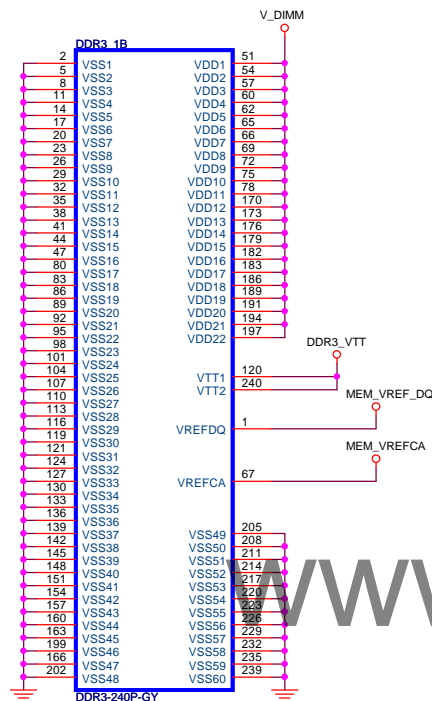
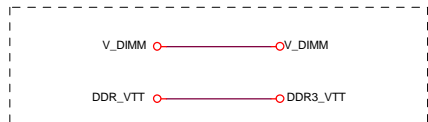


SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A4

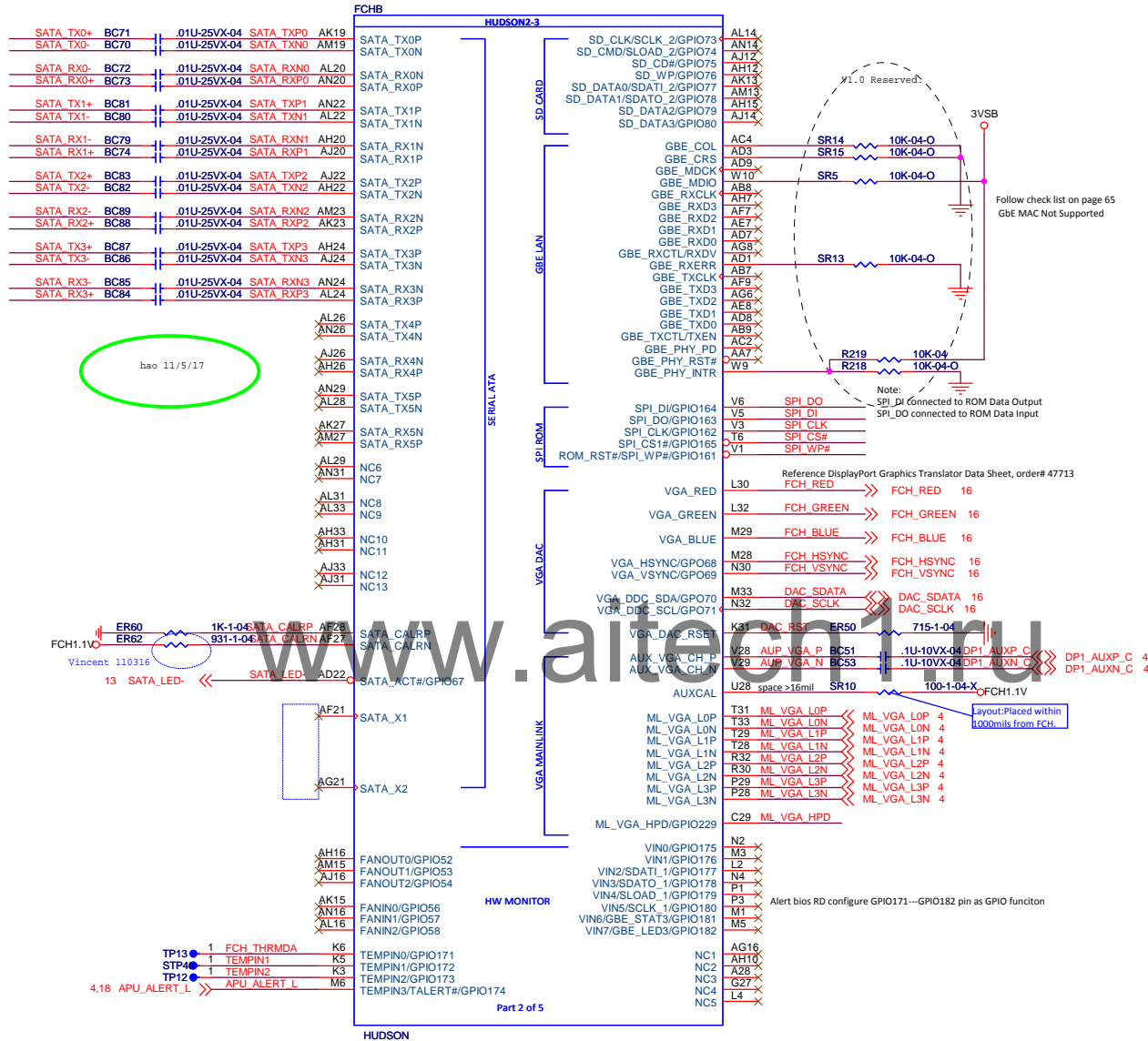
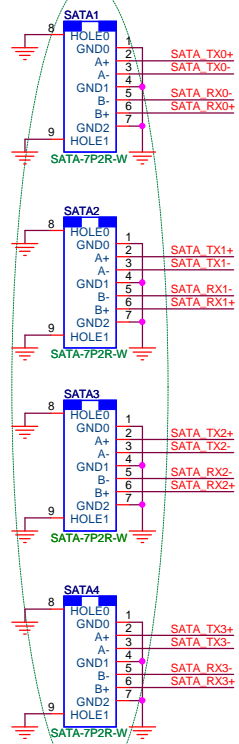
VCC3 >>> VCC3

Elitegroup Computer Systems	
Title DDR3 DIMM A & B CHANNEL	
Size Custom	Document Number A55F-M4
Date: Tuesday, September 27, 2011	Sheet 7 of 29

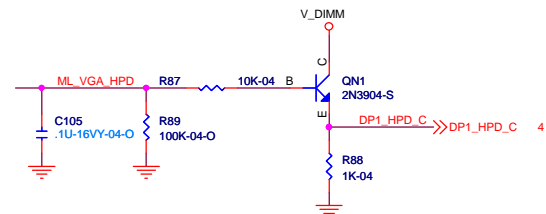
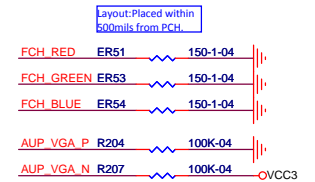
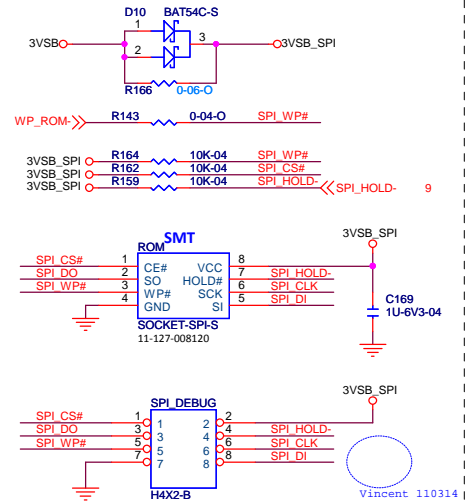


Layout: DIMM Slots placement

A0	
A1	C24, C25, BC30, BC31
B0	
B1	C26, C27, BC32, BC33

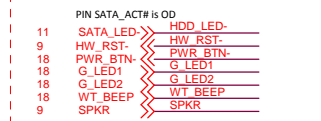


SPI ROM

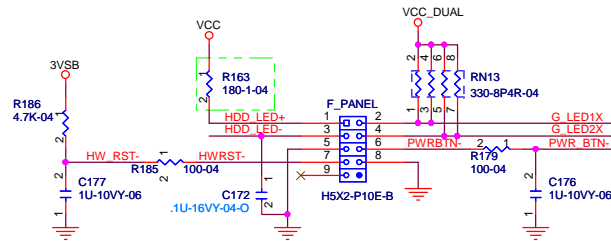


FRONT PANEL

External Connection



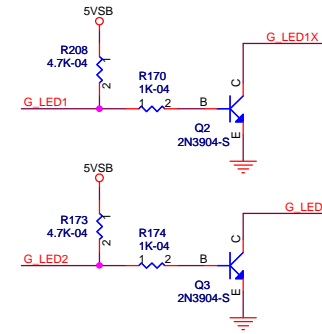
If you found anything wrong with this circuit, please contact with Jack Hu (Ext:26200)



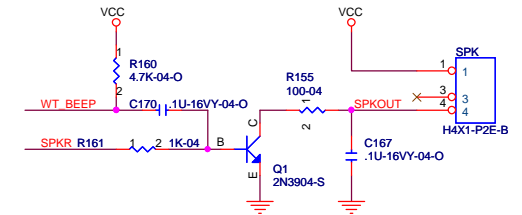
F_PANEL

F_PANEL

1	2	+	ISOLED
3	4		
5	6		
7	8		
9			

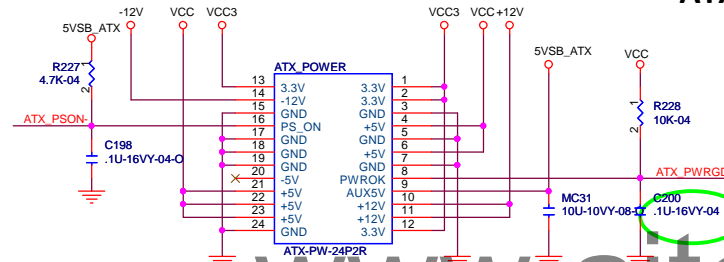
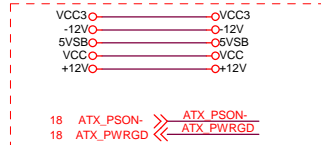


BUZZER/SPK

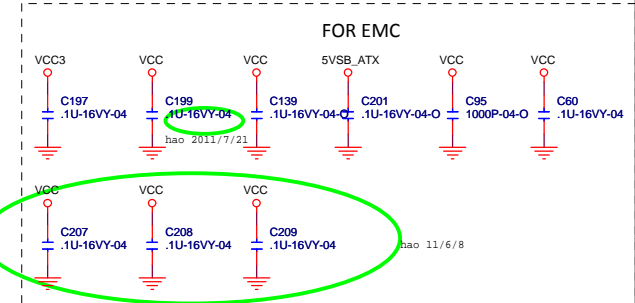
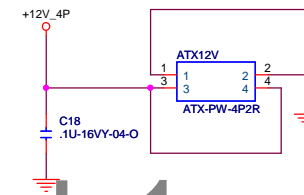


POWER CONNECTOR

External Connection

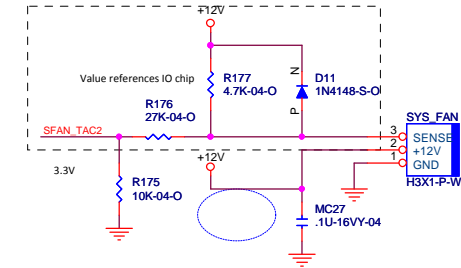
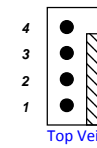
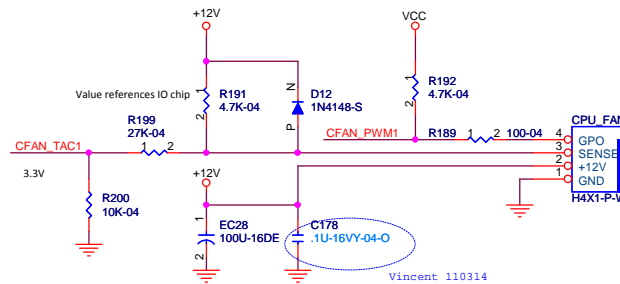


ATX_PWR

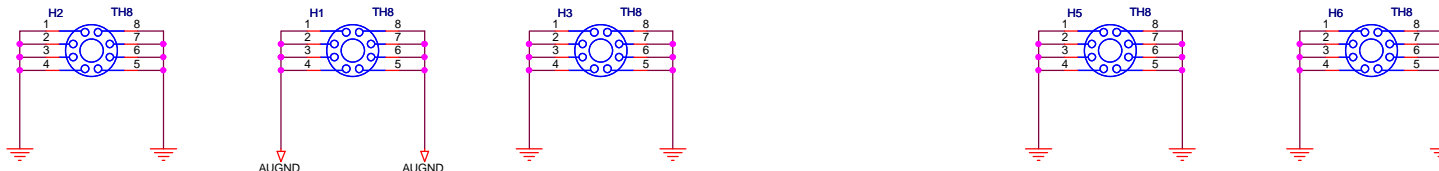


FAN

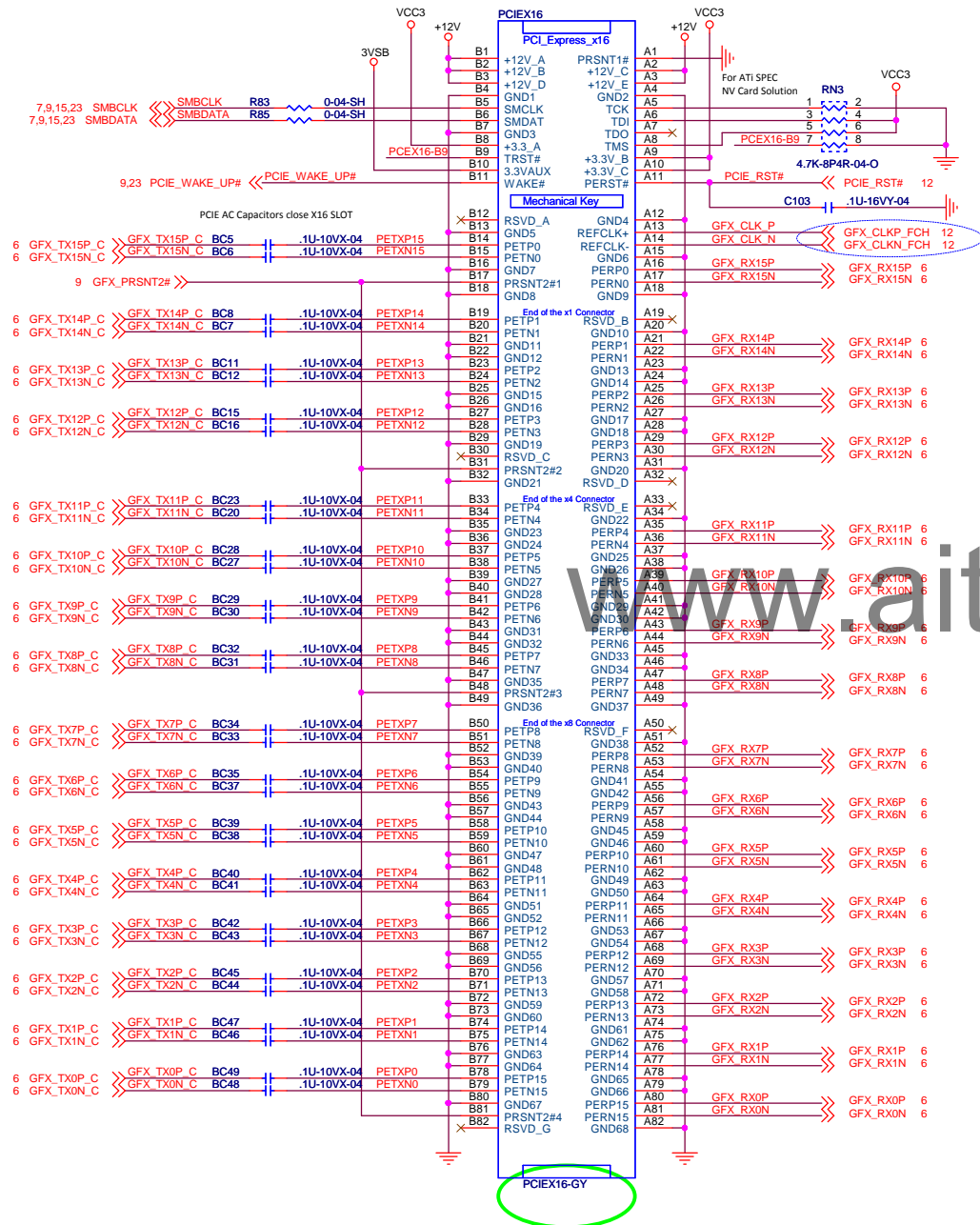
External Connection



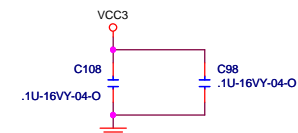
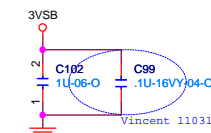
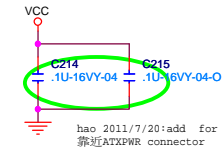
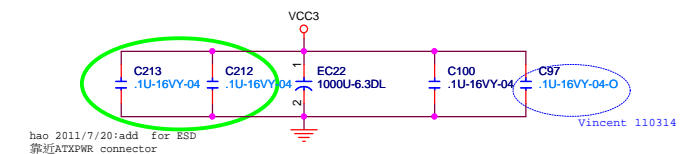
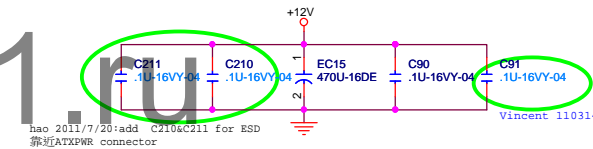
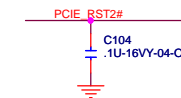
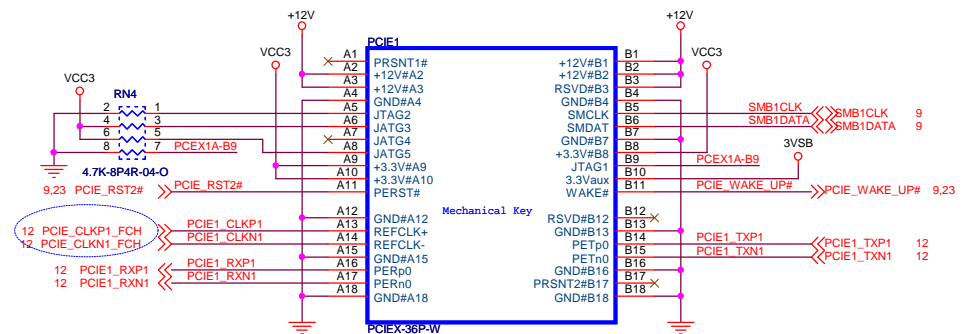
SCREW HOLES



PCI_EXPRESS_x16



PCI_EXPRESS_x1 A



PCI SLOT

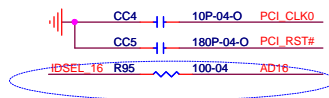
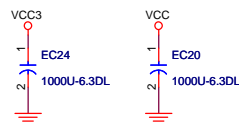
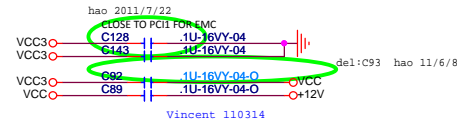
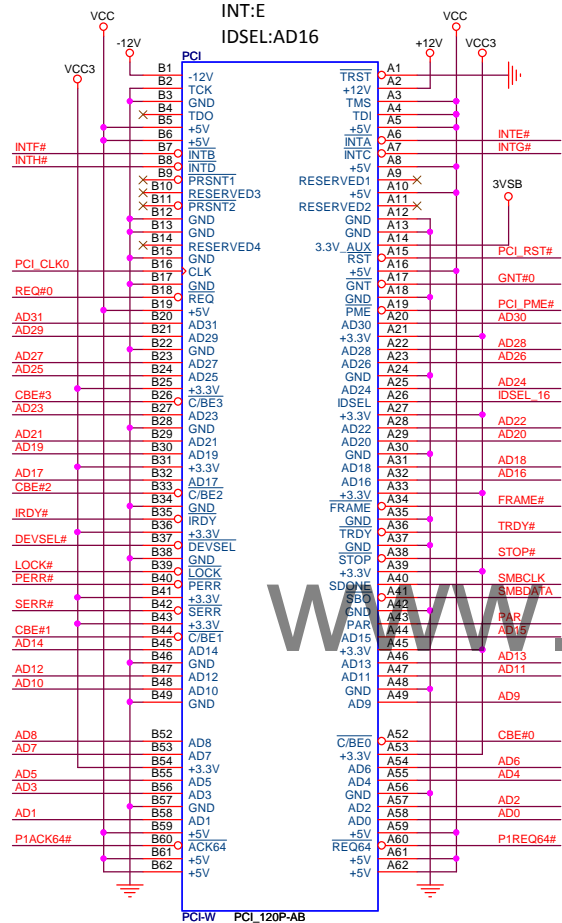
INT:E
IDSEL:AD16

del PCIEx1 B hao 11/5/17

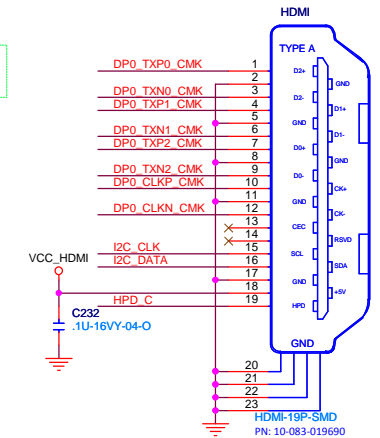
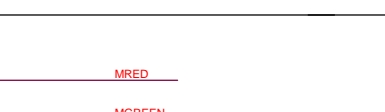
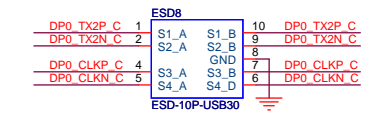
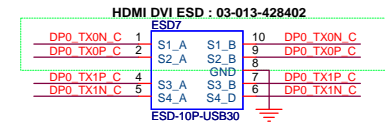
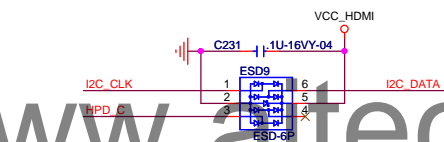
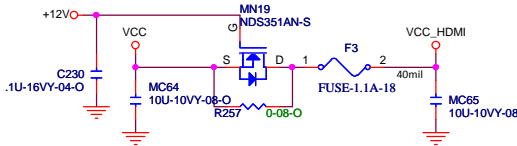
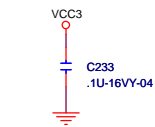
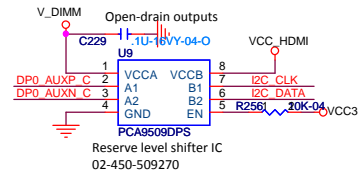
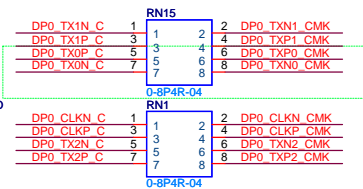
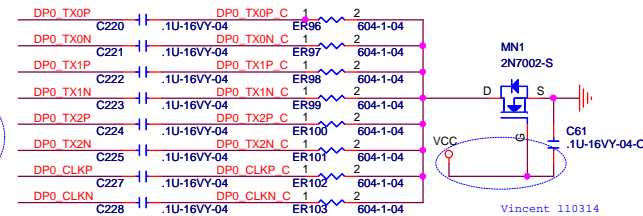
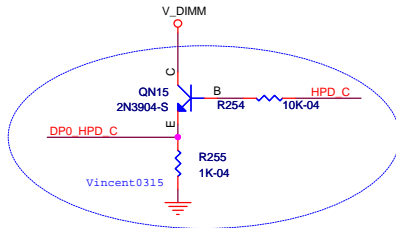
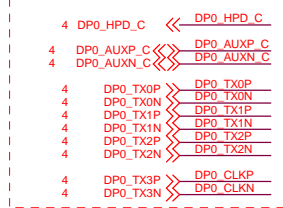
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External Connection

7,9,14,23	SMBCLK	SMBCLK
7,9,14,23	SMBDATA	SMBDATA
12	PCI_CLK0	PCI_CLK0
12	PCI_RST#	PCI_RST#
12	GNT#0	GNT#0
12	AD[0..31]	AD[0..31]
12	CBE#[0..3]	CBE#[0..3]
12	INTE#	INTE#
12	INTF#	INTF#
12	INTG#	INTG#
12	INTH#	INTH#
12	REQ#0	REQ#0
9	PCI_PME#	PCI_PME#
12	FRAME#	FRAME#
12	IRDY#	IRDY#
12	TRDY#	TRDY#
12	DEVSEL#	DEVSEL#
12	STOP#	STOP#
12	LOCK#	LOCK#
12	PERR#	PERR#
12	SERR#	SERR#
12	PAR	PAR



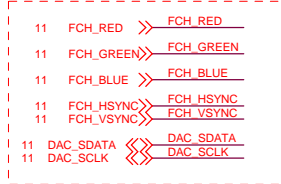
External Connection



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Add HDMI Willy 11/08/19

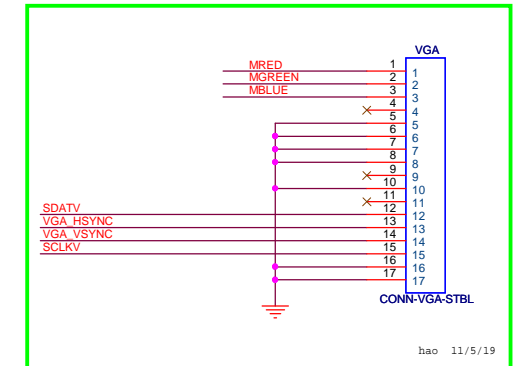
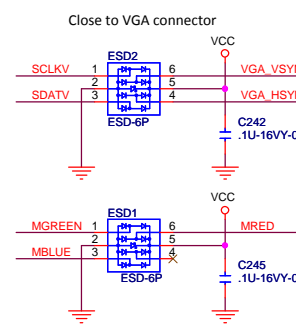
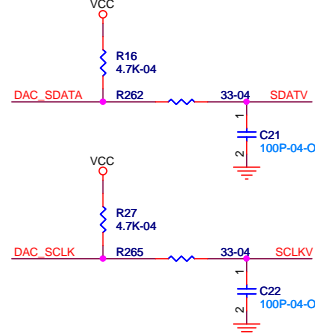
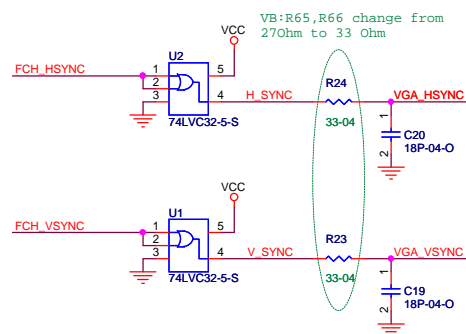
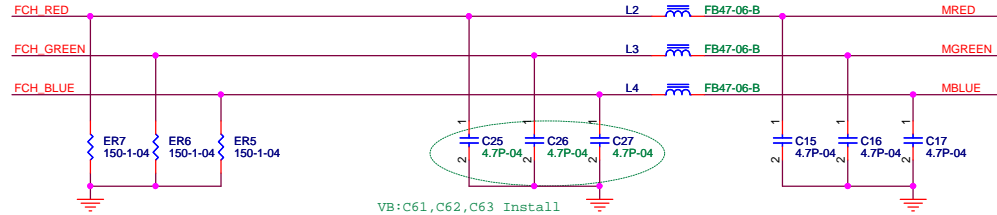
External Connection



Layout Guide:



VGA



External Connection



F_USB1



F_USB2

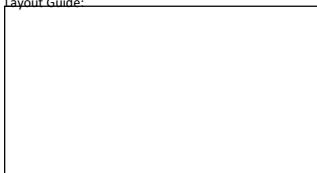
Vincent 110317



USB_2R

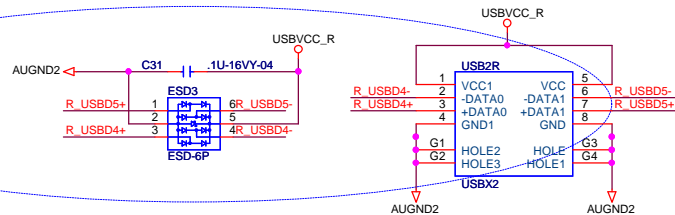
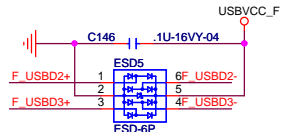
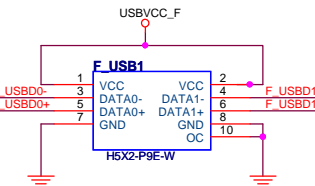


Layout Guide:



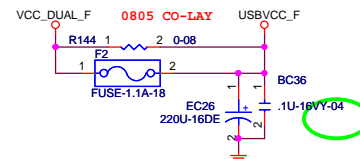
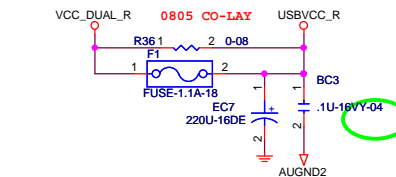
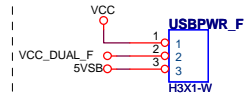
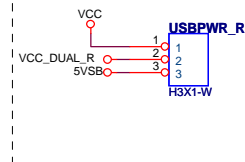
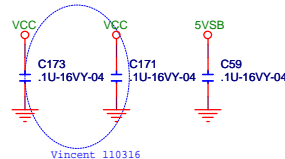
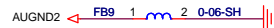
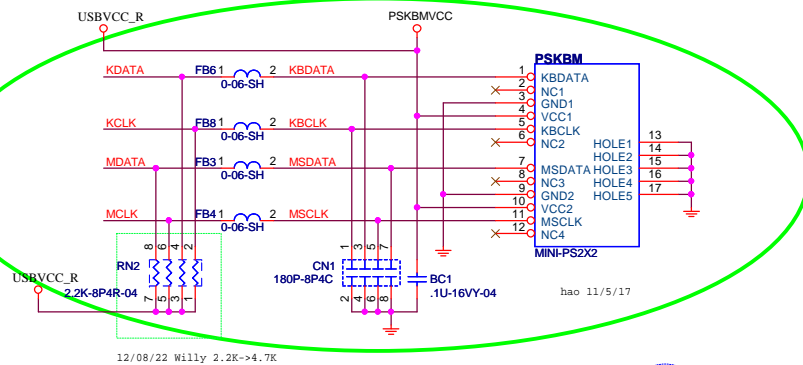
hao 11/5/24

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del F_USB3 hao 11/5/24

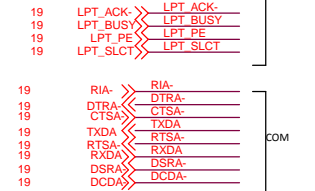
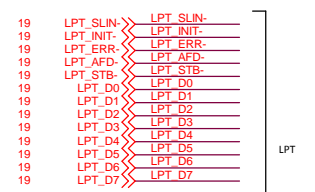
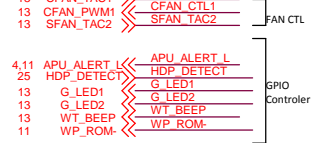
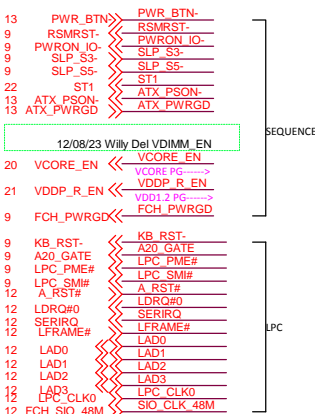


150 Mils Width

USBPWR_R1	USB POWER SELECT
1-2	VCC*
2-3	5VSB

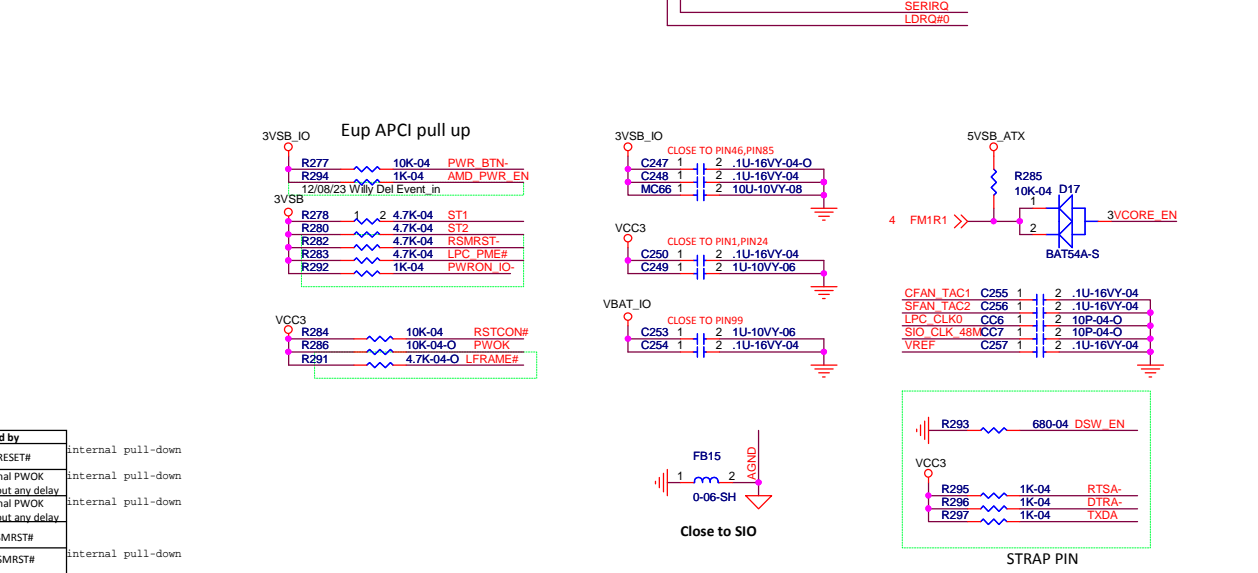
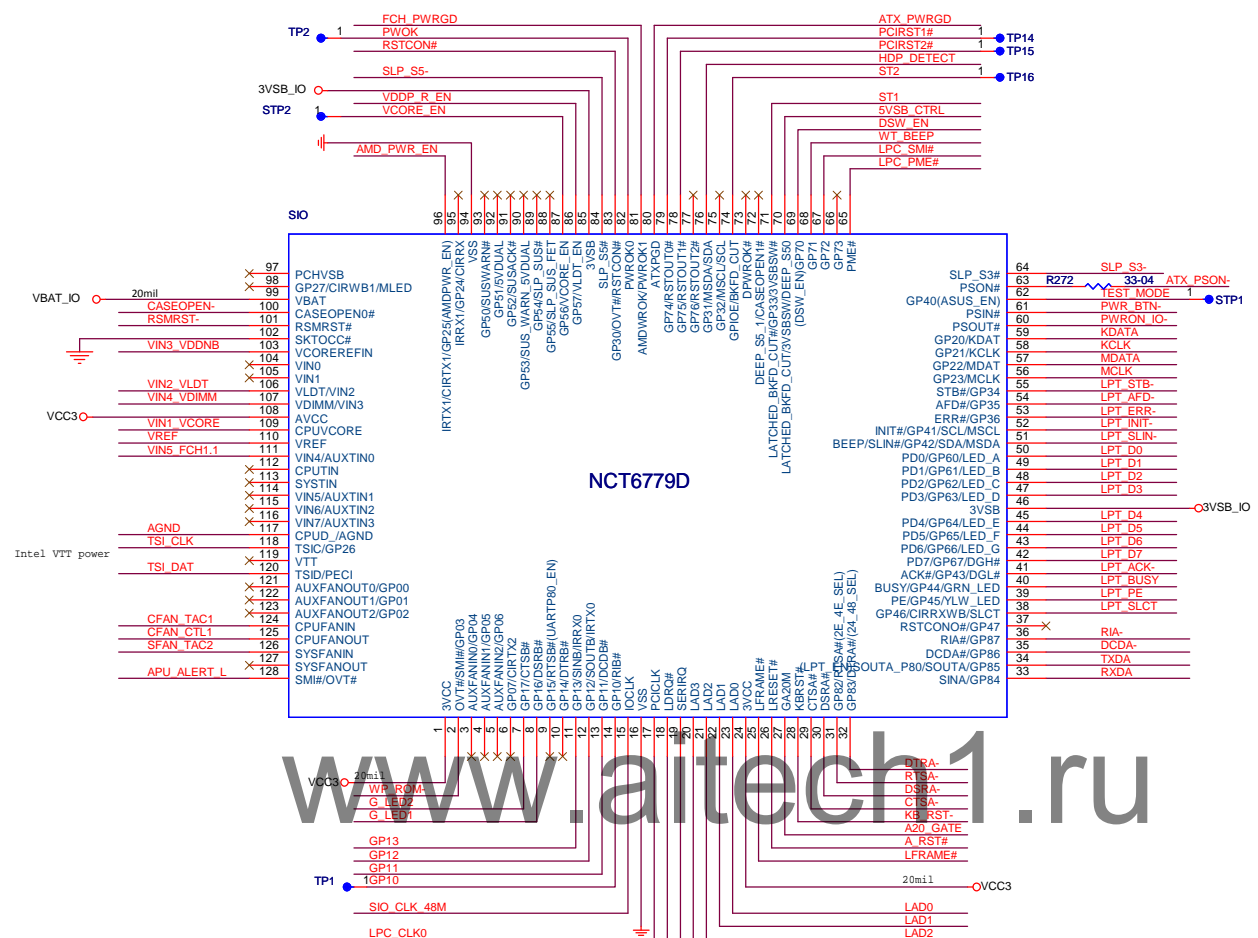
USB Switch-->USB jumper hao 11/5/19

External Connection

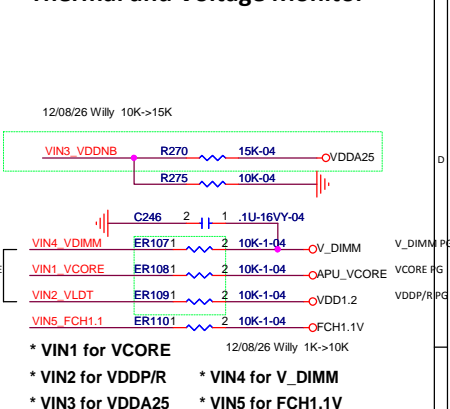


SIO STRAPPING

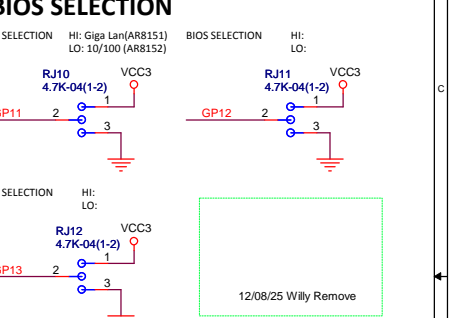
PIN	SYMBOL	VALUE	Description	Strapped by
31	SIO I/O	HI	Address=4E/4F	LRESET#
32	Address selection	LO	Address=2E/2F	
	Input_clk_sel	HI	CLK=48MHz	internal PWOK without any delay
34	LPT_EN	HI	EN_PRT function	internal PWOK without any delay
69	DSW_EN	HI	Strapped PIN 54,66-68,74,77	RSMRST#
96	AMDPWR_EN	HI	Strapped PIN 88-93	RSMRST#
		HI	EN_AMD PWR SEQUENCE	
		LO	DIS_AMD PWR SEQUENCE	



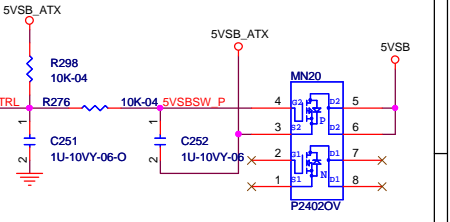
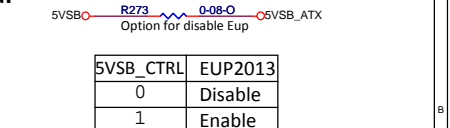
Thermal and Voltage Monitor



BIOS SELECTION



Eup



Elitegroup Computer Systems

SIO-NCT6779D

A55F-M4

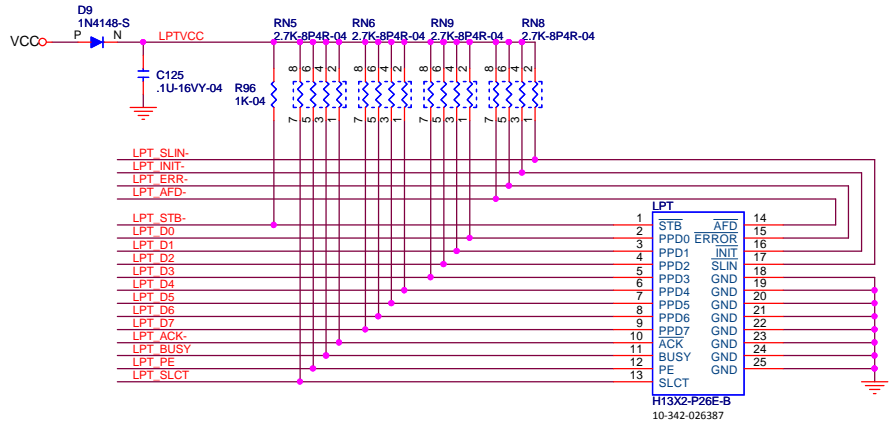
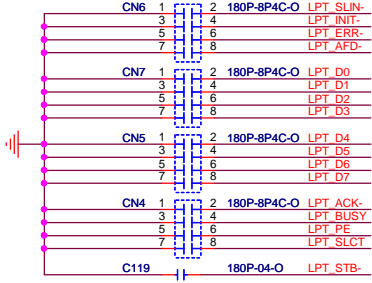
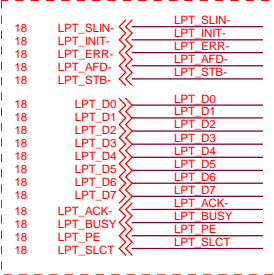
Rev A

Date: Tuesday, September 27, 2011

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LPT Header

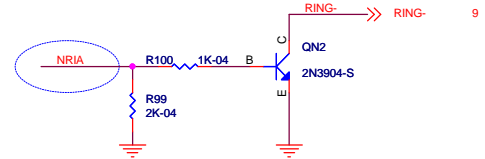
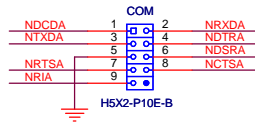
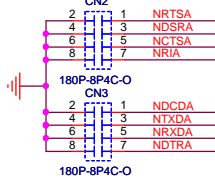
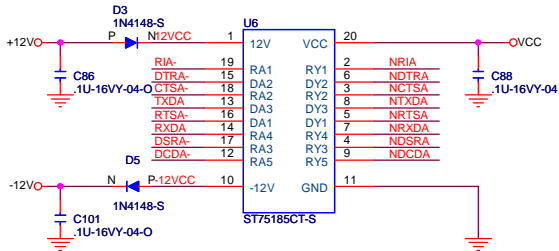
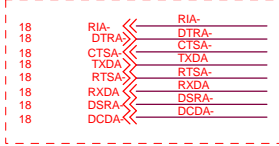
External Connection

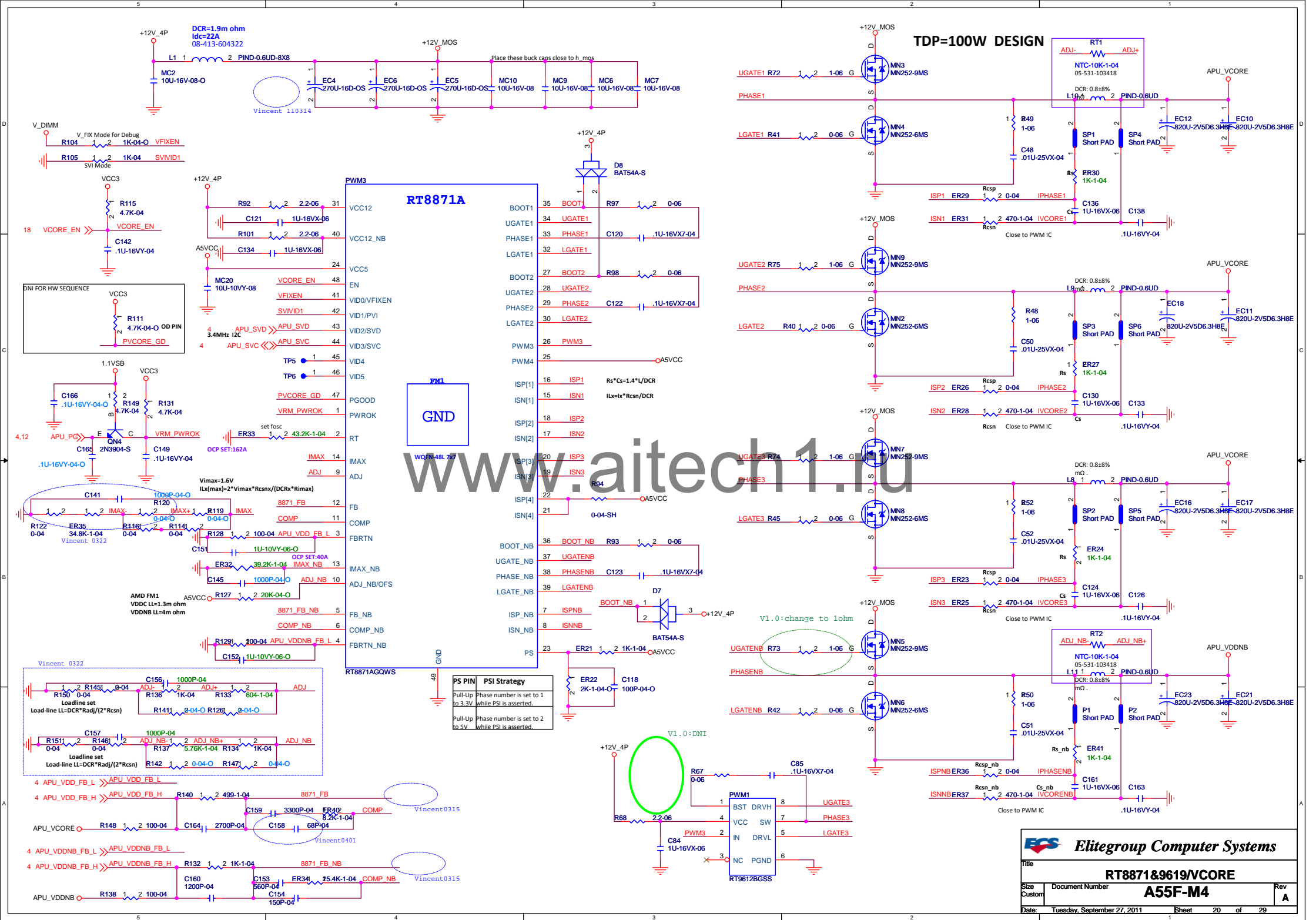


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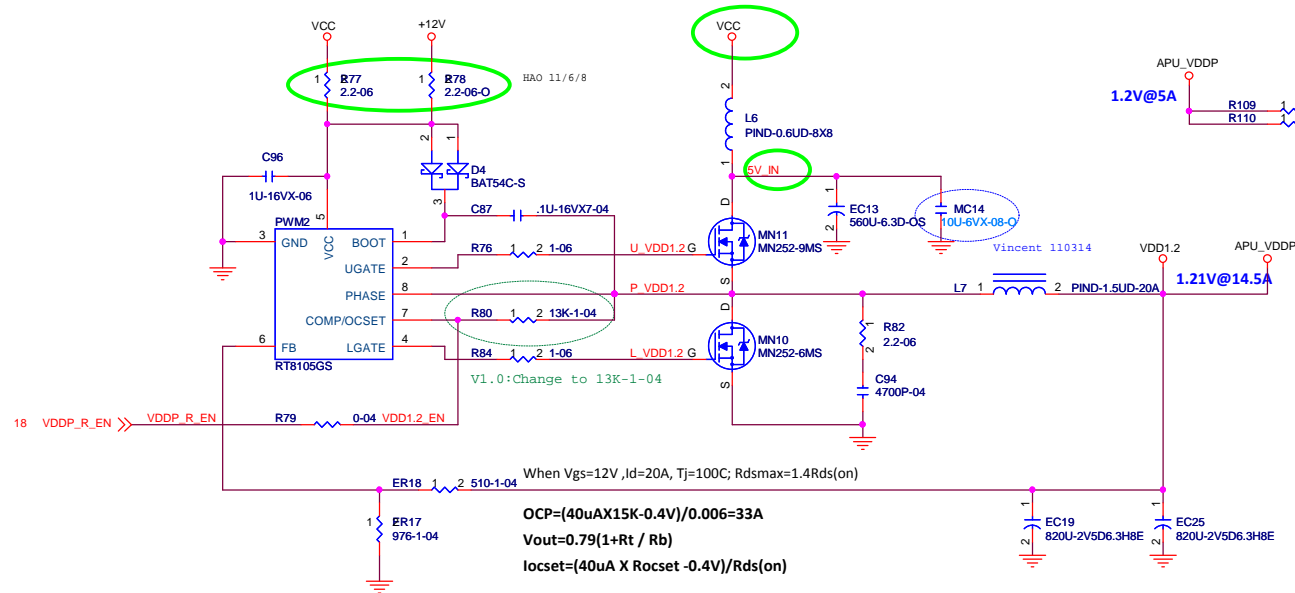
COM

External Connection

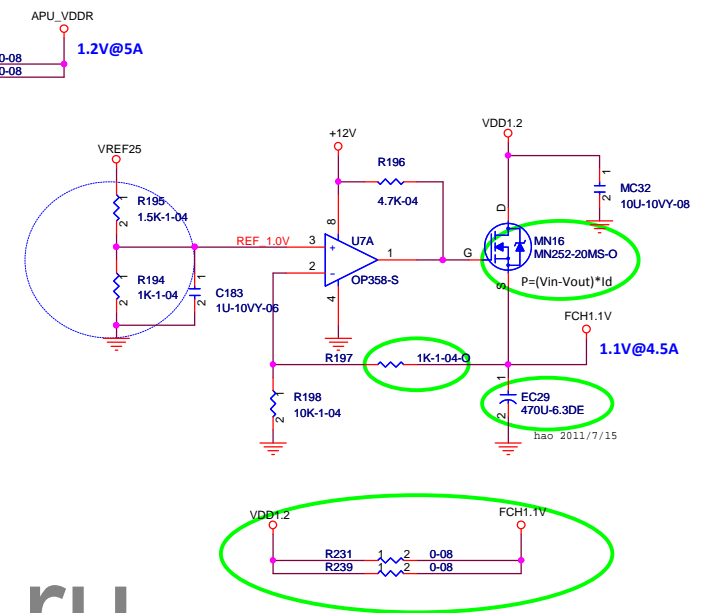




VDD1.2



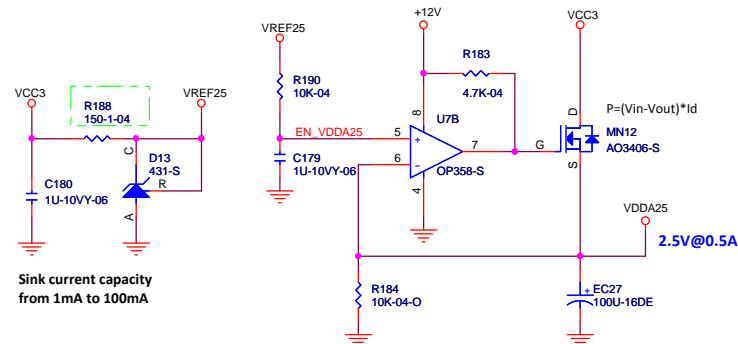
FCH1.1V



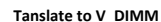
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Reserve for HW sequence

VDDA25



VCC_DUAL



V_DIMM=1.5~2.1V@21A
1pcs DDRIII@3A+APU_VDDIO@5.5A

1.6V@21A

hao 2011/7/22

When $V_{gs}=12V$, $I_d=20A$, $T_j=100^\circ C$; $R_{dsmax}=1.4R_{ds(on)}$

206 1 2 10-04

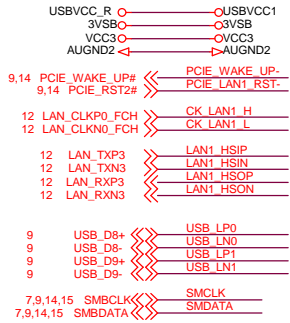
$$OCP = (40\mu A \times 17.4K - 0.4V) / 0.006 \times 1.4 = 35A$$
$$V_{out}=0.79(1+R_t / R_b)$$
$$I_{ocset} = (40\mu A \times R_{ocset} - 0.4V) / T_j R_{ds(on)}$$

4pcs dual DDR3@12A

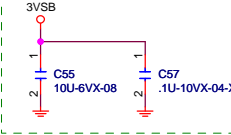
3VSB



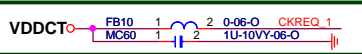
External Connection



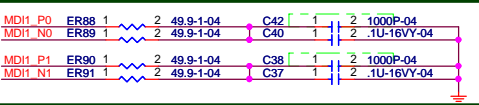
Closed To Pin1



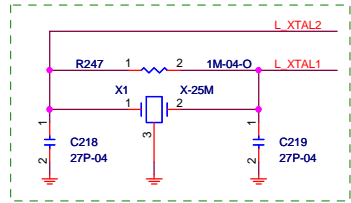
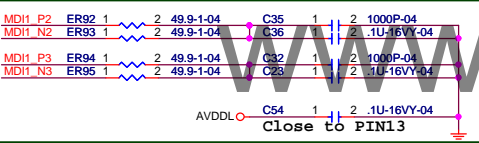
Ch



Ci



Cg

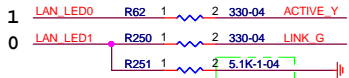


BOM Difference

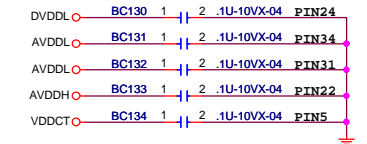
	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Cb	V	X	X
Cc	USB2-LAN-1000	USB2-LAN-100	USB2-LAN-1000
Cd	X	V	X
Ce	0-04	.010U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Cl	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

HW Strapping

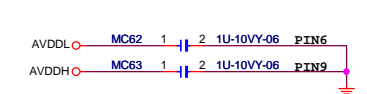
LED0 : 0 -> OC disable
1 -> OC enable
LED1 : 0 -> VDDCT_REG enable
1 -> VDDCT_REG disable



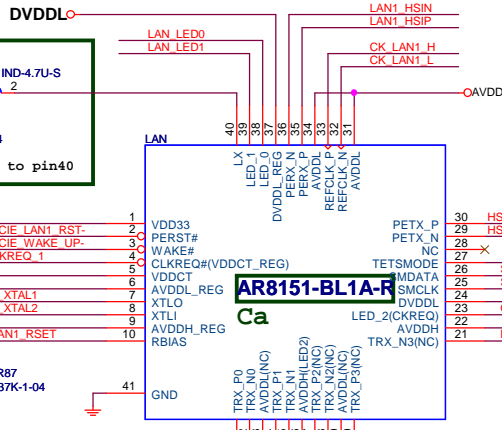
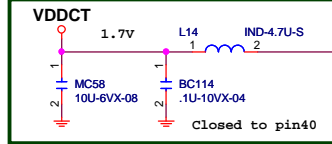
Closed To PWR Loading Pin



Closed To PWR Source Pin

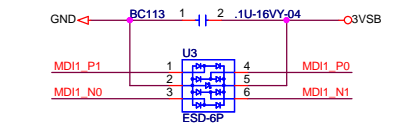
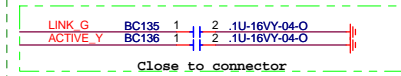


Cb

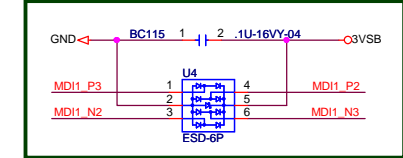


20100929
Change By Andy lu

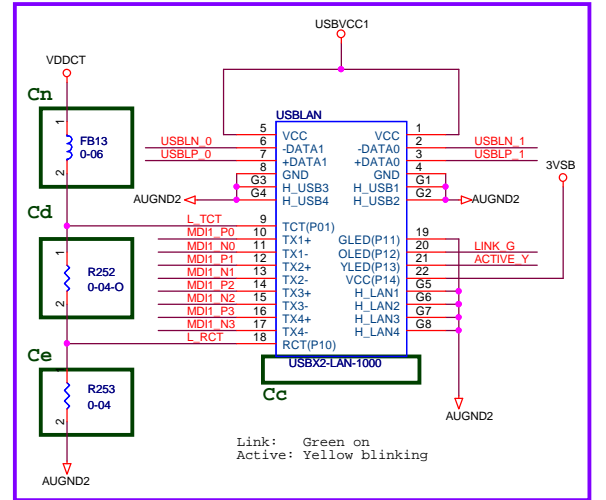
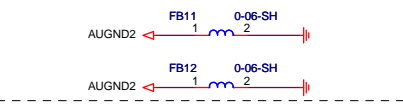
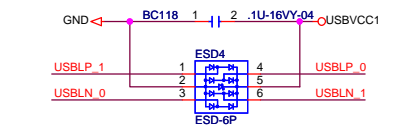
20110914
Willy Added for EMC



Cf



20100929
Short By Andy lu



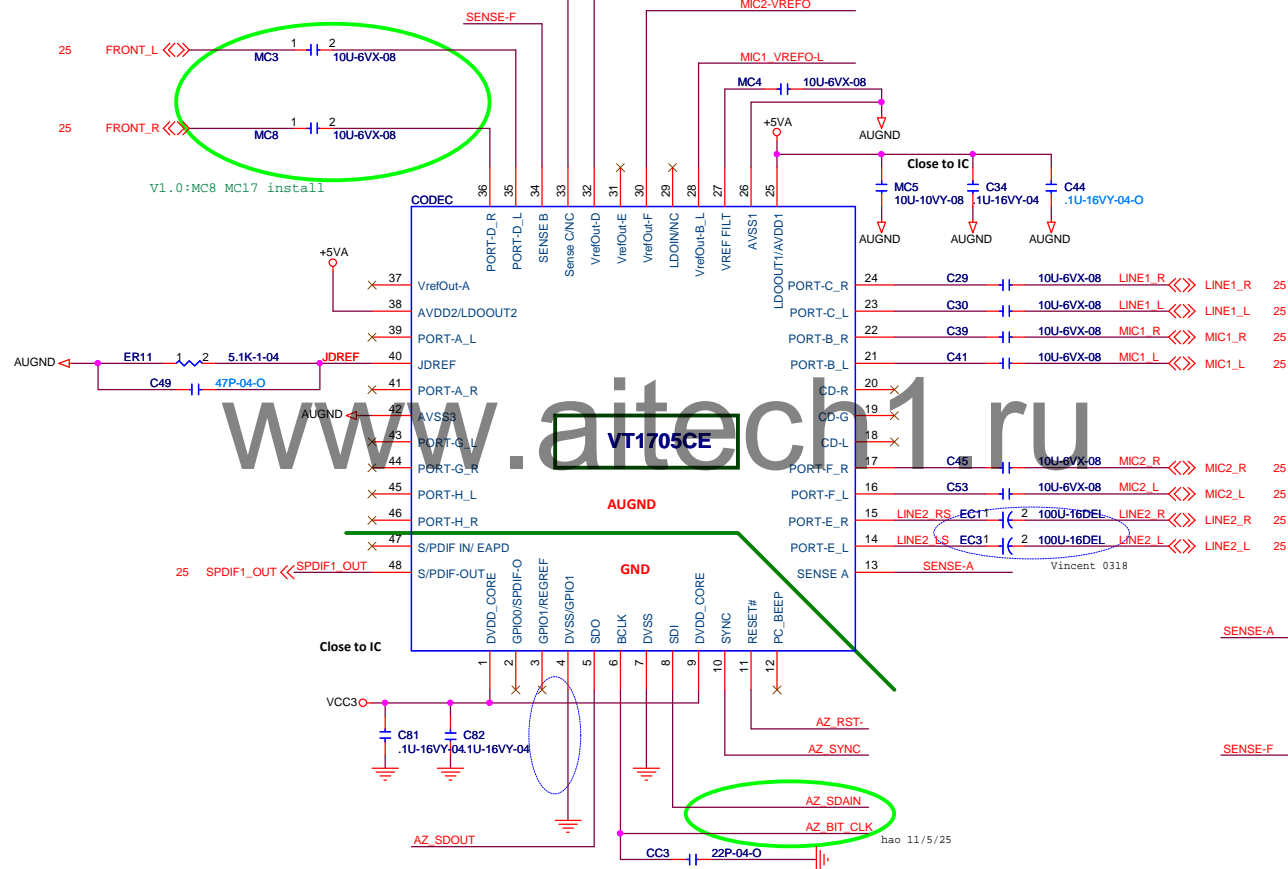
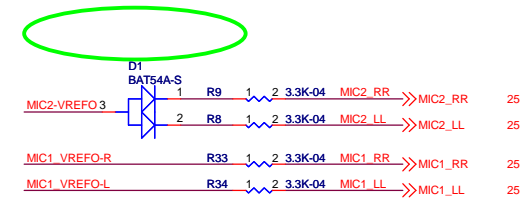
Link: Green on
Active: Yellow blinking

Elitegroup Computer Systems

Title	PCIE LAN AR8151-B/AR8152-B	Rev	A
Size	Document Number		
Custom	A55F-M4		
Date:	Tuesday, September 27, 2011	Sheet	23 of 29

Pin connections for the ADXL345 module:

- VCC3 to VCC3
- 5VSB to 5VSB
- +12V to +12V
- AZ_RST# to AZ_RST-
- AZ_BITCLK# to AZ_BIT_CLK
- AZ_SYNC# to AZ_SYNC
- AZ_SDIOIN to AZ_SDAIN
- AZ_SDOUT to AZ_SDOUT
- AUGND to AUGND




SENSE-A

Component	Value	Signal	Port
C67	47P-04-O	AUGND	
ER14	5.1K-1-04	FRONT_JD	25 PORT-D
ER13	10K-1-04	LINE1_JD	25 PORT-C
ER12	20K-1-04	MIC1_JD	25 PORT-B

SENSE-F

Component	Value	Signal	Port
ER9	20K-1-04	MIC2_JD	25 PORT-F
ER8	39.2K-1-04	LINE2_JD	25 PORT-E
C33	47P-04-O	AUGND	

Pin2 VT1705: GPIO(*)/SPDIFO ALC662: GPIO(*)	Pin3 VT1705: GPIO ALC662: GPIO(*)	Pin4 VT1705 : D-GND ALC662 : D-GND
---	---	--

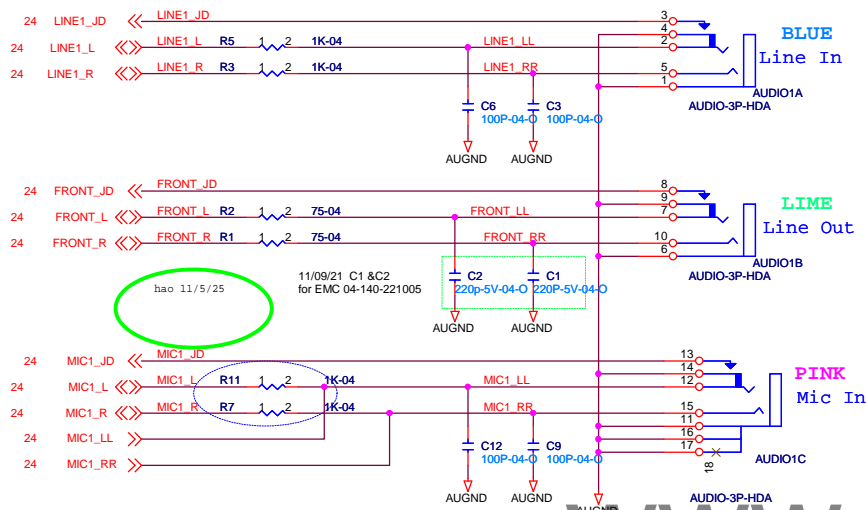
 Elitegroup Computer Systems			
Title			
CODEC VT1705CE			
Size	Document Number	A55F-M4	Rev
Custom			A
Date:	Tuesday, September 27, 2011	Sheet	24 of 29

External Connection

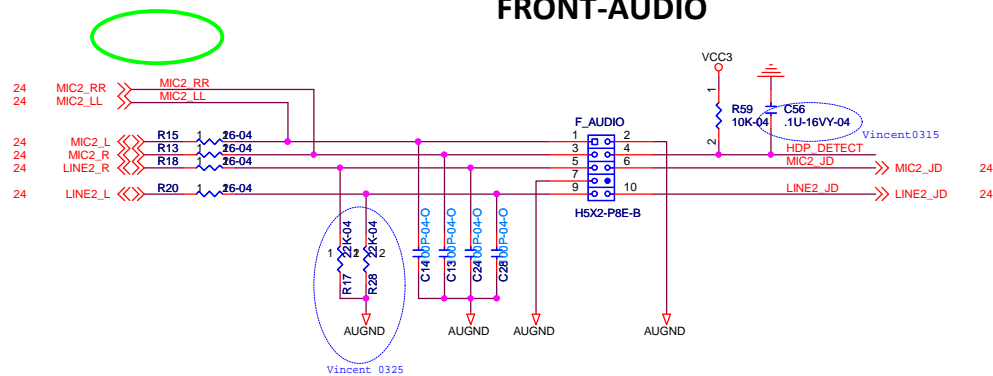
18 HDP_DETECT << HDP_DETECT

* HDP_DETECT connect to SIO or SB GPIO for AC97 Panel support

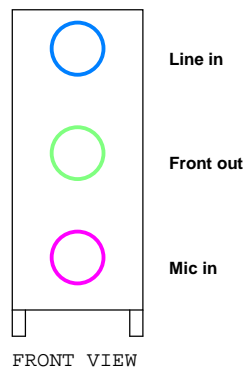
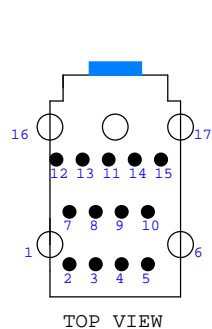
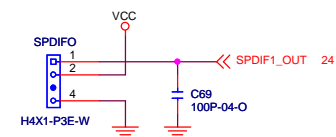
REAR-AUDIO



FRONT-AUDIO



SPDIF OUT



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ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX8P
12V +/-5%

Switching RT8871 3+1 phases

0.8~1.55V 100A Max.

0.8~1.55V 31.25A Max.

Switching RT8105

1.2V 14A Max.

Linear OP358

2.5V 0.75A Max.

Switching RT8105

1.5V 22A Max.

1/2 Divider RT9173

0.75V 1A Max.

Linear OP358

1.1V 4.5A Max.

Converter APL5336

1.1VSB D3:1.230A/D2:0.524A

LDO APL1085

3.3VSB 2A

LDO 3904

5VDUAL Switch IC UP7536

5VDUAL Switch IC UP7536

5VDUAL Switch IC UP7536

7805

PCI Slots per	
5V	5A
3.3V	7.6A
3.3Vaux	0.375A
12V	0.5A
-12V	0.1A

Total 1 Slot

X16 PCIe Slot per	
3.3V	3A
3.3Vaux	0.375A
12V	5.5A

Total 1 Slot

X1 PCIe Slot per	
3.3V	3A
3.3Vaux	0.375A
12V	0.5A

Total 2 Slot

USB2.0 Headers	
5VDUAL	3A

Total 6 Ports

USB2.0 Conn.	
5VDUAL	3A

Total 6 Ports

USB3.0 HEADER	
5VDUAL	1.8A

Total 2 Ports

LAN RTL8111E-VL/8105E-VL		
VDD3P3	3.3V	194mA


AUDIO ALC662-VC/892		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

AMD APU FM1		
VDD CORE	VID 0.5 ~ 1.55V	TDC 80A
VDD NB	VID 0.5 ~ 1.55V	TDC 25A
VDDIO	1.5V	5.5A
VDDR	1.2V	5.0A
VDDP	1.2V	5.0A
VDDA	2.5V	0.5A

DDR3 UDIMM x4		
VDDQ	1.5V	15A (S0) 1A (S3)
DDR_VTT	0.75V	1A

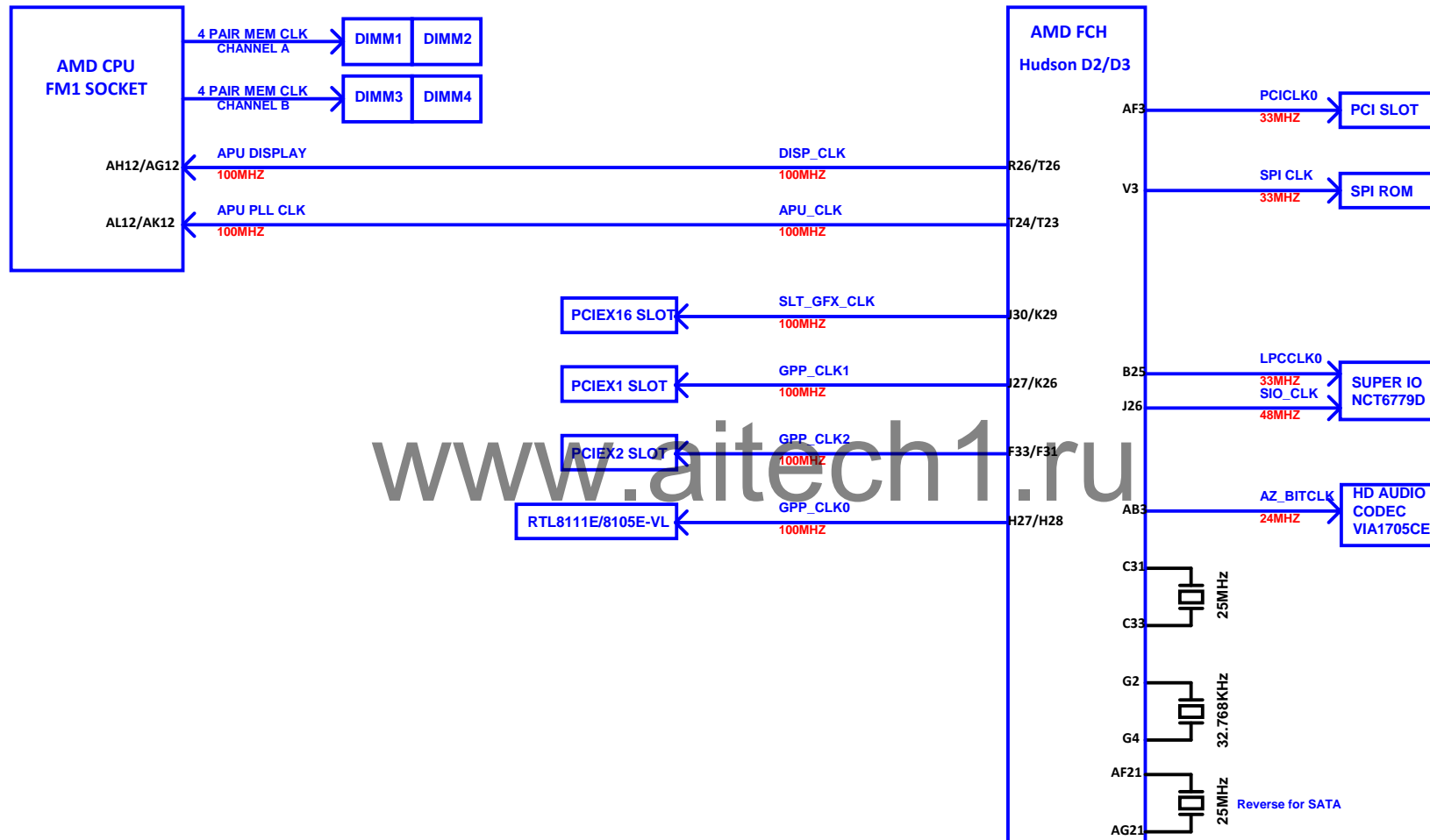
AMD HUSDSO-N-D2/D3		
VDDCR_11	1.1V	1.414A
VDDAN_11_CLK	1.1V	0.340A
VDDAN_11_PCIE	1.1V	1.088A
VDDAN_11_SATA	1.1V	1.337A
VDDAN_11_ML	1.1V	0.226A
VDDPL_11_DAC	1.1V	0.007A
VDDIO_33_PCIGP	3.3V	0.102A
VDDPL_33_*	3.3V	0.132A
VDDCR/AN_11_USB_S	1.1V	0.182A
VDDCR_11_S	1.1V	0.272A
VDDPL_11_SYS_S	1.1V	0.070A
VDDCR/AN_11_SUSB_S	1.1V	0.706A
VDDIO_33_S	3.3V	0.059A
VDDAN/PL_33_USB_S	3.3V	0.484A
VDDXL_33_S	3.3V	0.005A
VDDIO_AZ_S	3.3V	0.026A
VDDAN_33_HWM_S	3.3V	0.012A
VDDBT_RTC	3V	<4uA

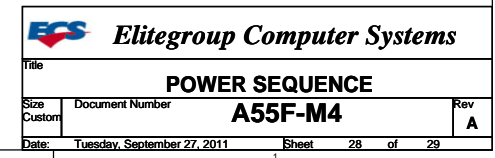
SUPER I/O NCT6779D		
BAT 3.3V	3.3V	~25uA
3VSB_IO	3.3V	~8mA
AVCC(VCC3)	3.3V	~25mA


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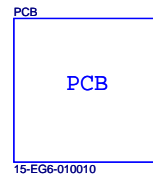
Title			Rev A
POWER DELIVERY CHART			
Size Custom	Document Number A55F-M4		
Date:	Tuesday, September 27, 2011	Sheet	26 of 29

CLOCK DISTRIBUTION

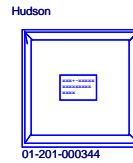




PCB Stackup

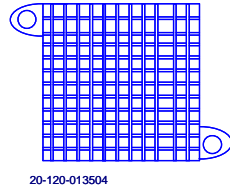


PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

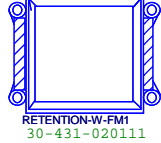


104 item

FCH(104) 36, 2x12x12, 2



CPU(104)



ROM(104)



CLR_CMOS(1-2)



USBPWR_F(1-2)



USBPWR_R(1-2)



BT(104)



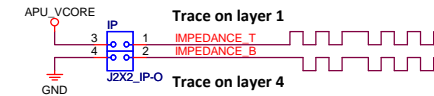
X3(wire)(103)



PCB Impedance control			
Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg
60	5 (20/5/20)	6	2116
50	4 (50/4/50)	6	1080
42	6 (50/6/50)	6	1080

1)Circuit type 1

Layer 1:TOP
Layer 2:PWR
Layer 3:GND
Layer 4:BOTTOM



Notes:

- 1). "PWR" net means inner power plane under impedance trace.
- 2). "GND" net means inner ground plane under impedance trace.
- 3). IP1 footprint is J2X2_IP
- 4). After netlist running, please specially take care the single net name: "IMPEDANCE_T" and "IMPEDANCE_B".

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